The following listing of claims will replace all prior versions and listings of claims in this divisional application:

LISTING OF CLAIMS

Claims 1-23. (Canceled)

Claim 24. (Original) A method for manufacturing a single electron memory device including a single electron storage element in a gate lamination pattern formed on a nano-scale channel region of a MOSFET, wherein formation of the gate lamination pattern comprises:

(a) sequentially forming a lower layer and a single electron storage medium for storing a single electron tunneling through the lower layer on a substrate;

(b) forming an upper layer including a plurality of quantum dots on the single electron storage medium;

(c) forming a gate electrode layer on the upper layer to be in contact with the plurality of quantum dots; and

(d) patterning the lower layer, the single electron storage medium, the upper layer, and the gate electrode layer, in reverse order.

Claim 25. (Original) The method as claimed in claim 24, wherein the formation of the upper layer comprises:

forming a first upper layer on the single electron storage medium;

forming the plurality of quantum dots on the first upper layer; and

forming a second upper layer to cover the plurality of quantum dots on the first upper layer.

Claim 26. (Original) The method as claimed in claim 24, wherein the formation of the gate electrode layer further comprises polishing the upper layer until the plurality of quantum dots are exposed before forming the gate electrode layer on the upper layer.

Claim 27. (Original) The method as claimed in claim 25, wherein the formation of the gate electrode layer further comprises polishing the second upper layer

until the plurality of quantum dots are exposed before forming the gate electrode layer on the second upper layer.

Claim 28. (Original) The method as claimed in claim 24, wherein the formation of the upper layer further comprises:

forming the plurality of quantum dots on the single electron storage medium; and

forming the upper layer to cover the plurality of quantum dots on the single electron storage medium.

Claim 29. (Original) The method as claimed in claim 28, wherein the formation of the gate electrode layer further includes polishing the upper layer until the plurality of quantum dots are exposed before forming the gate electrode layer on the upper layer.

Claim 30. (Original) The method as claimed in claim 24, wherein the single electron storage medium is formed of a material selected from the group consisting of silicon nitride (Si_3N_4), PZT, silicon (Si), silicon germanium (SiGe), gallium arsenide (GaAs), and a metal.

Claim 31. (Original) The method as claimed in claim 24, wherein the plurality of quantum dots contact the single electron storage medium and a bottom surface of the gate electrode.

Claim 32. (Original) The method as claimed in claim 24, wherein the plurality of quantum dots are formed by method selected from the group consisting of a selective growth method, a self-assembled growth method and a nano-scale lithography method.

Claim 33. (Original) A method for manufacturing a single electron memory device including a single electron storage element in a gate lamination pattern

formed on a nano-scale channel region of a MOSFET, wherein the formation of the gate lamination pattern comprises:

(a) forming a lower layer on a substrate;

(b) forming an upper layer including a plurality of vertically spaced-apart first and second quantum dots on the lower layer;

(c) forming a gate electrode on the upper layer to be in contact with the plurality of second quantum dots; and

(d) patterning the lower layer, the upper layer, and the gate electrode, in reverse order.

Claim 34. (Original) The method as claimed in claim 33, wherein the formation of the upper layer comprises:

forming the plurality of first quantum dots on the lower layer, to store a single electron tunneling through the lower layer;

forming a first upper layer having a thickness sufficient to cover the plurality of first quantum dots;

forming the plurality of second quantum dots on the first upper layer; and

forming a second upper layer to cover the plurality of second quantum dots on the first upper layer.

Claim 35. (Original) The method as claimed in claim 34, wherein the formation of the gate electrode comprises polishing the second upper layer until the plurality of second quantum dots are exposed before forming the gate electrode on the second upper layer.

Claim 36. (Original) The method as claimed in claim 34, wherein the lower layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

Claim 37. (Original) The method as claimed in claim 34, wherein the first upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

Claim 38. (Original) The method as claimed in claim 34, wherein the second upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), and titanium oxide (TiO_2).

Claim 39. (Original) The method as claimed in claim 34, wherein the gate electrode is formed of a material selected from the group consisting of doped Si, doped SiGe, doped GaAs, a metal, a silicide, and a polycide.

Claim 40. (Original) The method as claimed in claim 34, wherein the plurality of quantum dots are formed of silicon.

Claim 41. (Original) The method as claimed in claim 34, wherein the plurality of quantum dots are formed by a method selected from the group consisting of a selective growth method, a self-assembled growth method and a nano-scale lithography method.

Claim 42. (Original) A method for manufacturing a single electron memory device including a single electron storage element in a gate lamination pattern formed on a nano-scale channel region of a MOSFET, wherein the formation of the gate lamination pattern comprises:

(a) forming a lower layer on a substrate;

(b) sequentially forming a single electron storage means for storing a single electron tunneling through the lower layer, and an upper layer covering the single electron storage means, on the lower layer, wherein the surface of the upper layer is uneven;

(c) forming a gate electrode layer on the upper layer; and

(d) patterning the lower layer, the single electron storage means, the upper layer, and the gate electrode layer, in reverse order.

Claim 43. (Original) The method as claimed in claim 42, wherein the single electron storage means is a single electron storage medium and is formed of a material selected from the group consisting of silicon nitride (Si_3N_4), silicon (Si), PZT, silicon germanium (SiGe), gallium arsenide (GaAs), and a metal.

Claim 44. (Original) The method as claimed in claim 42, wherein the single electron storage means is a plurality of quantum dots.

Claim 45. (Original) The method as claimed in claim 42, wherein the lower layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

Claim 46. (Original) The method as claimed in claim 42, wherein the upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

Claim 47. (Original) The method as claimed in claim 42, wherein the gate electrode is formed of a material selected from the group consisting of doped Si, doped SiGe, doped GaAs, a metal, a silicide, and a polycide.

Claim 48. (Original) The method as claimed in claim 42, wherein the plurality of quantum dots are formed of silicon.

Claim 49. (Original) The method as claimed in claim 42, wherein the lower layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

Claim 50. (Original) The method as claimed in claim 42, wherein the upper layer is formed of a material selected from the group consisting of silicon oxide (SiO_2), alumina (Al_2O_3), tantalum oxide (TaO_2), titanium oxide (TiO_2), HfO_2 and ZrO_2.

Claim 51. (Original) The method as claimed in claim 42, wherein the gate electrode is formed of a material selected from the group consisting of doped Si, doped SiGe, doped GaAs, a metal, a silicide, and a polycide.

Claim 52. (Original) The method as claimed in claim 44, wherein the plurality of quantum dots are formed of silicon.

Claim 53. (Original) The method as claimed in claim 44, wherein the plurality of quantum dots are formed by a method selected from the group consisting of a selective growth method, a self-assembled growth method and a nano-scale lithography method.